



VIGNAN'S LARA INSTITUTE OF TECHNOLOGY & SCIENCE

(Approved by AICTE & Affiliated to JNTUK, Kakinada; An ISO 9001:2015 Certified Institution)
Vadlamudi, Chebrolu (Mandal), Guntur (Dist.) - 522 213.

Department of Electronics and Communication Engineering

VLITS/ECE/WORKSHOPS/2019/015

Date:021.0.2019

Circular

All the staff and students are here by informed that a A Two-day workshop on "PCB Layout Design Using Proteus ARES" is scheduled on 03-01-2019&05-01-2019and so all are informed to attend the workshop without fail and can gain knowledge with hands on experience.

Venue:Old Block Seminar Hall,programming lab

Time: 9.00am to 5.00pm

Experts:Mr.R.Jishnu,Sr.Engineer, Pantech Solution &Mr.E.Bala Vignesh,Sr.Engineer,
Pantech Solutions

M. S. Rao

HoD, ECE

Head

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